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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,456	06/10/2005	Padraig Omathuna	US02 0615 US	3794
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NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER PARIKH, KALPIT	
			ART UNIT 2187	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/538,456

Applicant(s)

OMATHUNA, PADRAIG

Examiner

KALPIT PARIKH

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-18 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 10 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

The instant detailed action is in response to Applicant's submission filed on 10 June 2005.

I. APPLICATION INFORMATION

Application No. 10538456 has a total of 18 claims pending in the application; there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **CLAIMS 1-13,15-18** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584).

As per claim 1, Yamada discloses a method of transferring programming instructions from a first memory disposed on a substrate, to a plurality of integrated circuits (ICs), comprising:

- a first one of the plurality of ICs (see Yamada FIG 1: 1 MASTER CPU) accessing the first memory (see FIG 6: S2), retrieving a first set of programming instructions, and

storing the first set of programming instructions within the first one of the plurality of ICs (see Yamada FIG 6: S3 and COL 3 LINES 32-46); and

- the first one of the plurality of ICs accessing the first memory integrated circuit, retrieving a second set of programming instructions, and transmitting the second set of programming instructions to a second one of the plurality of ICs (see Yamada FIG 6: S5 and COL 3 LINES 32-46).

However, Yamada does not expressly disclose the memory and the plurality of integrated circuit (ICs) are disposed on the substrate.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

As per claim 2, Yamada in view of Stancil disclose the method of Claim 1,

- wherein the first and second ones of the plurality of ICs each comprise a processor capable of executing, respectively, the first and second sets of programming instructions (see Yamada FIG 6: S3, S5: 'PROGRAM DATA').

As per claim 3, Yamada in view of Stancil disclose the method of Claim 2, further comprising

- the first one of the plurality of ICs executing at least a portion of the first set of programming instructions (see Yamada COL 3 LINES 45-55).

As per claim 4, Yamada in view of Stancil disclose the method of Claim 3,

- wherein executing at least a portion of the first set of programming instructions occurs prior to transmitting the second set of programming instructions to a second one of the plurality of ICs (see Yamada FIG 6: S3, S5).

As per claim 5, Yamada in view of Stancil disclose the method of Claim 2,

- further comprising the first one of the plurality of ICs accessing the first memory, retrieving a first set of data, and storing the first set of data within the first one of the plurality of ICs; and the first one of the plurality of ICs accessing the first memory, retrieving a second set of data, and transmitting the second set of data to a second one of the plurality of ICs (see Yamada FIG 6: S3, S5).

As per claim 6, Yamada in view of Stancil disclose the method of Claim 3,

- wherein the substrate comprises a printed circuit board (see Stancil COL 2 LINE 25: "motherboard").

As per claim 7, Yamada in view of Stancil disclose the method of Claim 3,

- wherein transmitting comprises serially shifting data out from the first integrated circuit and concurrently shifting data in to the second integrated circuit (see Yamada FIG 6: S5 "SERIALLY TRANSFER").

As per claim 8, Yamada in view of Stancil disclose the method of Claim 7,

- further comprising transmitting control information from the first integrated circuit to the second integrated circuit prior to transmitting the second set of programming instructions to a second one of the plurality of ICs (see Yamada FIG 6: S4).

As per claim 9, Yamada in view of Stancil disclose the method of Claim 8,

- wherein the control information directs the second one of the plurality of ICs to receive a subsequent transmission of programming instructions (see Yamada FIG 6: S5).

As per claim 10, Yamada discloses in a system including a plurality of integrated circuits (ICs), each IC comprising a memory for storing at least programming instructions, each further comprising a processor coupled to the memory for executing programming instructions stored in the memory; the system further including a single non-volatile memory disposed on the printed circuit board and coupled for memory access to only a first one of the plurality of ICs, a method of downloading code from the single non-volatile memory to each of the plurality of ICs, comprising:

- receiving, at a first one of the plurality of ICs, a first set of data from the single non-volatile memory; storing the first set of data in the memory of the first one of the plurality of ICs (see Yamada FIG 6: S3 and COL 3 LINES 28-46);
- receiving, at the first one of the plurality of ICs, a second set of data from the single non-volatile memory; transmitting the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs; and storing the second set of data in the memory of the second one of the plurality of ICs; wherein the first and second sets of data comprise program code (see Yamada FIG 6: S5 and COL 3 LINES 28-46).

However, Yamada does not expressly disclose the plurality of ICs disposed on a printed circuit board.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance systems (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

As per claim 11, Yamada in view of Stancil discloses the method of Claim 10,

- further comprising: executing, in the first IC, at least a portion of the code in the program first set of data (see FIG 6: S6);
- receiving, at the first one of the plurality of ICs, a third set of data from the single non-volatile memory; transmitting the third set of data from the first one of the plurality of ICs to a third one of the plurality of ICs; and storing the third set of data in the memory of the third one of the plurality of ICs (see Stancil FIG 2: 114, 116, 118);

As per claim 12, Yamada in view of Stancil disclose the method of Claim 10,

- wherein transmitting the second set of data from the first one of the plurality of ICs to the second one of the plurality of ICs comprises serially shifting data out of the first one of the plurality of ICs via an output terminal; wherein the output terminal is

coupled to an input terminal of the second one of the plurality of ICs, the input terminal coupled to circuitry within the second one of the plurality of ICs that is adapted to receive serial data (see Yamada FIG 6: S5 SERIALLY).

As per claim 13, Yamada in view of Stancil disclose the method of Claim 12,

- further comprising providing transmitting control information from the first one of the plurality of ICs to the second one of the plurality of ICs prior to transmitting the second set of data (see Yamada FIG 6: S4).

As per claim 15, Yamada discloses an electronic product, comprising: a first integrated circuit having a first processor (see Yamada FIG 1: 1), a first internal memory (see Yamada FIG 1: 3), a first serial communication interface (see Yamada FIG 1: "SERIAL COMMUNICATION"), and an external memory interface (see Yamada FIG 1: 4); an external memory coupled to the external memory interface (see FIG 1: 5 MEMORY CARD); a second integrated circuit having second processor (see FIG 1: 6), a second internal memory (see FIG 1: 8), and a second serial communication interface, the second serial communication interface being coupled to the first serial communication interface (see FIG 1: "SERIAL COMMUNICATION");

However, Yamada does not expressly disclose wherein the first integrated circuit, the external memory, and the second integrated circuit are disposed on a substrate.

In the same field of endeavor Stancil discloses it is well known to place many components on a motherboard (substrate) (see Stancil COL 5 LINES 5-10).

It would have been obvious to modify Yamada to integrate the components on a motherboard.

The suggestion/motivation for doing so would have been of higher performance system s (see Stancil COL 2 LINES 24-28).

Therefore it would have been obvious to modify Yamada to integrate the components on a motherboard for the benefit higher performance to arrive at the invention as specified in the claims.

As per claim 16, Yamada in view of Stancil disclose the electronic product of claim 15,

- wherein the first processor is coupled to the first internal memory, the first internal memory is adapted to receive a first code image (see Yamada FIG 6: S3), the second processor is coupled to the second internal memory, the second internal memory is adapted to receive a second code image (see FIG 6: S5), and the external memory is a non-volatile memory encoded with the first and second code images (see COL 2 LINES 50-57).

As per claim 17, Yamada in view of Stancil disclose the electronic product of claim 16,

- wherein the first integrated circuit includes a first hardware facility for performing at least a first function, and the second integrated circuit includes a second hardware facility for performing at least a second function, and the first and second functions are different (see COL 3 LINES 24-45).

As per claim 18, Yamada in view of Stancil disclose the electronic product of Claim 17, further comprising

- a third integrated circuit, having a third processor, a third internal memory, and a third serial communication interface, the third serial communication interface being coupled to the second serial communication interface, the third processor coupled to the third

internal memory, the third internal memory is adapted to receive a third code image, and the external memory further encoded with the third code image (see Stancil FIG 2: 114, 116, 118).

[Stancil discloses configuring plural processing devices using a single EEPROM.]

3. **CLAIM 14** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Pat No. 5757639) in view of Stancil (US Pat No. 6272584) as applied to claim 13 above, and further in view of May (US Pat No. 7343483).

As per claim 14, Yamada in view of Stancil disclose the method of claim 13.

However, Yamada in view of Stancil do not expressly disclose wherein the control information is transmitted in accordance with a JTAG standard of communication.

In the same field of endeavor May discloses using a JTAG standard of communication (see May FIG 2: PLD JTAG).

It would have been obvious to modify Yamada in view of Stancil to use JTAG standard of communication.

The suggestion/motivation for doing so would have been for the benefit of using an industry standard protocol (see May COL 3 LINES 40-45).

Therefore it would have been obvious to use the JTAG standard of communication for the benefit of an industry standard communication protocol to arrive at the invention as specified in the claims.

III. CLOSING COMMENTS

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

IIIa. CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-18 have received a first action on the merits and are subject of a non-final office action.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

IV. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KALPIT PARIKH whose telephone number is (571)270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin L. Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KLE/kp /KP/
10 May 2009

/Brian R. Peugh/
Primary Examiner, Art Unit 2187